REMARKS

Claims 1, 3, 5, 6 and 21-25 are pending in the present application. Claim 1 has been amended. Claims 2, 4 and 7-12 have been canceled. Claims 21-25 have been presented herewith.

Drawings

Applicant notes the Examiner's acceptance of the Replacement drawing as submitted along with the Amendment dated June 6, 2007.

Claim Rejections-35 U.S.C. 112

Claims 1-12 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

Claim 1 has been amended to improve antecedent of the data. Also, the combining circuit of claim 1 is featured as receiving the first output data from the arithmetic logic unit and the second output data from the register, and outputting combined data which is provided by replacing a part of the second output data with a part of the first output data. It should thus be clear that the combining circuit performs replacing so as to provide the outputted combined data. Claim 1 has been further amended to include the features of claim 2, wherein a part of the second output data and a part of the first output data is more clearly featured. Applicant respectfully submits that claims 1, 3, 5 and 6 as pending are in compliance with 35 U.S.C. 112,

second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

Applicant also notes that in compliance with 37 C.F.R. 1.121(c)(2), the text of any deleted matter must be shown by strike-through, except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The claim amendments are thus in compliance with 37 C.F.R. 1.121(c)(2).

Claim Rejections-35 U.S.C. 101

Claims 1-12 have been rejected under 35 U.S.C. 101 as allegedly being directed to non-statutory subject matter. The Examiner has apparently asserted that all the claims are directed to an apparatus for merely performing manipulations and calculations of data values, and that in order for such a claimed invention to be statutory, the claimed invention must accomplish a practical application by transforming an article or physical object to a different state or thing, or produce a useful, concrete and tangible result. This rejection is respectfully traversed for the following reasons.

The arithmetic unit of claim 1 includes in combination among other features a memory for storing data; an arithmetic logic unit "for executing a predetermined arithmetic operation with respect to the data from the memory to provide the first output data, the data being grouped into one of several patterns"; a register for temporarily storing data; and a combining circuit that replaces a part of second output data with a part of first output data. Claim 1 is thus clearly directed to a machine (apparatus), and

thus falls within one of the four enumerated categories of patentable subject matter recited in 35 U.S.C. 101.

In accordance with the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility as set forth in 1300 OG 142, the first step in determining whether a claim is directed to statutory subject matter under 35 U.S.C. 101 is to identify whether the claim falls within one of the four enumerated categories of patentable subject matter recited in section 101 (process, machine, manufacture or composition of matter). If the claim **does not fall** within one of the four enumerated categories of patentable subject matter, the analysis then proceeds to the steps of considering Judicial Exceptions, Practical Application, and Preemption. On the other hand, if the claim **does fall** within one of the four enumerated categories of patentable subject matter, **the claim is deemed as directed to statutory subject matter in compliance with 35 U.S.C. 101, and the analysis is thus concluded**.

As asserted above, the apparatus of claim 1 is an arithmetic unit and features in combination physical components such as a memory, an arithmetic logic unit, a register and a combining circuit. Since claim 1 clearly is a "machine" (apparatus), claim 1 falls within one of the four statutory categories, and thus is directed to eligible subject matter under 35 U.S.C. 101. That is, the arithmetic unit of claim 1 is not a literary work, is not rules to play a game, is not a legal agreement, is not a signal per se, and is not a computer program, which all fall outside one of the enumerated statutory categories under section 101.

The Examiner's requirement on page 3 of the current Office Action dated August 24, 2007, that the claims must accomplish a practical application or a useful, concrete and tangible result, is incorrect and irrelevant, because claim 1 clearly falls within one of the four statutory categories of eligible subject matter under 35 U.S.C. 101. That is, these requirements would apply as considered with respect to the Practical Application step as described in the Interim Guidelines, as noted above. However, since claim 1 clearly falls within one of the four enumerated categories of patentable subject matter, consideration of the Practical Application step of the test is unnecessary.

Accordingly, Applicant respectfully submits that claims 1, 3, 5 and 6 as pending are directed to statutory subject matter and thus are in compliance with 35 U.S.C. 101. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

Claim Rejections-35 U.S.C. 102

Claims 1 and 3 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Getzlaff et al. reference (U.S. Patent No. 5,754,875).

Claim Rejections-35 U.S.C. 103

Claims 5 and 6 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Getzlaff et al. reference. Claims 4, 7 and 9-12 have been

rejected under 35 U.S.C. 103(a) as being unpatentable over the Getzlaff et al. reference in further view of the Shiell reference (U.S. Patent No. 6,408,320).

As noted above, claim 1 has been amended to include the features of claim 2. Claim 1 thus includes in combination among other features that "when the part of the second output data is replaced with the part of the first output data, the combining circuit shifts a position of data to be replaced in the second output data by a predetermined number of bits every time an operation process is executed". Although not necessarily limited thereto, these features may be understood in view of the patterns shown in Fig. 13 of the present application. The prior art as relied upon by the Examiner does not disclose these features. Applicant therefore respectfully submits that the arithmetic unit of claim 1 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that the above noted rejections, insofar as they may pertain to claims 1, 3, 5 and 6, are improper for at least these reasons.

Claims 21-25

The arithmetic unit of claim 21 includes in combination among other features a memory; an arithmetic logic unit; a register and a combining circuit "that carries out an operation process by receiving the first output data from the arithmetic logic unit and the second output data from the register, replacing a part of the second output data from

the register with a part of the first output data from the arithmetic logic unit based on the pattern of the data from the memory to provide combined data, and outputting the combined data to the memory for storage".

The Examiner has characterized the node after ALU 10 in Fig. 2 of the Getzlaff et al. reference as the combining circuit of the claims. However, ALU 10 and operand registers ORA and ORB 12 and 13 in Fig. 2 of the Getzlaff et al. reference each provide 32-bit data to the node subsequent ALU 10 along respective signal lines 17, 282 and 283, and the data are combined to provide 64-bit data along signal line 285. The node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference does not replace a part of data from operand registers 12 and 13 with a part of data from ALU 10 to provide combined data that is subsequently output to a memory for storage. No partitioning and replacement of data is accomplished specifically by the node subsequent ALU 10 in Fig. 2 of the Getzlaff et al. reference. Applicant therefore respectfully submits that claims 21-25 distinguish over the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to December 24, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.

/Andrew J Telesz Jr/

Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740